METAL GATE STACK AND SEMICONDUCTOR GATE STACK FOR CMOS DEVICES

FIELD OF THE INVENTION

[0001] The present invention generally relates to semiconductor devices, and particularly to complementary metal-oxide-semiconductor (CMOS) devices having a metal gate stack transistor and a semiconductor gate stack transistor, and methods of manufacturing the same.

BACKGROUND OF THE INVENTION

[0002] Complementary metal oxide semiconductor (CMOS) integration requires two gate materials, one having a work function near the valence band edge of the semiconductor material in the channel and the other having a work function near the conduction band edge of the same semiconductor material. In CMOS devices having a silicon channel, a conductive material having a work function of about 4.0 eV is necessary for n-type metal oxide semiconductor field effect transistors (NMOSFETs) and another conductive material having a work function of about 5.0 eV is necessary for p-type metal oxide semiconductor field effect transistors (PMOSFETs).

[0003] In conventional CMOS devices employing polysilicon gate materials, a heavily p-doped polysilicon gate and a heavily n-doped polysilicon gate are employed to address the needs. In CMOS devices employing high-k gate dielectric materials, suitable materials satisfying the work function requirements are needed. So far, identification of materials for a dual work function metal gate electrode system has presented some challenges. In particular, a high-k material metal gate stack for p-type field effect transistors that is capable of withstanding a high temperature thermal cycling encountered during a conventional semiconductor processing sequence has proven to be illusive so far.

[0004] Due to the difficulties encountered in providing suitable materials for a pair of dual work function metal gate electrode system, hybrid implementation of a high-k metal gate and a conventional polysilicon gate has been known in the art, in which a high-k material metal gate is employed for one type of transistors, i.e., n-type field effect transistors, and a conventional polysilicon gate is employed for another type of transistors, i.e., p-type field effect transistors. However, integration of the two types of gate electrodes introduces difficulties since the two types of gates have different requirements for spacer structures. On one hand, a low-k dielectric spacer or an oxide spacer is desirable on a polysilicon gate electrode to reduce parasitic capacitance between the polysilicon gate electrode and the source and drain regions. On the other hand, a high-k material metal gate requires protection of the high-k material from subsequent oxidation since an unstable oxygen content in the high-k gate dielectric degrades or introduces uncertainty in the dielectric constant of the high-k material.

[0005] In view of the above, there exists a need for a semiconductor structure providing a high-k material metal gate and a semiconductor gate electrode, while providing stability of the composition of the high-k material as well as a low parasitic capacitance for the semiconductor gate electrode, and methods of manufacturing the same.

SUMMARY OF THE INVENTION

[0006] The present invention addresses the needs described above by providing a CMOS structure including a diffusion barrier layer directly on the sidewalls a high-k material metal gate electrode and a low-k spacer directly on the sidewalls of a semiconductor gate electrode, and methods of manufacturing the same.

[0007] A semiconductor gate stack comprising a silicon oxide based gate dielectric and a doped semiconductor material is formed on a semiconductor substrate. A high-k material metal gate electrode comprising a high-k gate dielectric and a metal gate portion is also formed on the semiconductor substrate. Oxygen-impermeable dielectric spacers are formed on the sidewalls of the semiconductor gate stack and the high-k material metal gate stack. The oxygen-impermeable dielectric spacer on the semiconductor gate stack is removed, while the oxygen impermeable dielectric spacer on the high-k material metal gate electrode is preserved. A low-k dielectric spacer is formed on the semiconductor gate stack, which provides a low parasitic capacitance for the device employing the semiconductor gate stack.

[0008] According to an embodiment of the present invention, a semiconductor structure is provided, which comprises a high-k material metal gate structure and a semiconductor gate structure,

wherein the high-k material metal gate structure includes:

[0009] a high dielectric constant (high-k) material portion having a dielectric constant greater than 8.0 and located on a semiconductor substrate;

[0010] a metal gate portion comprising a metal and vertically abutting the high-k material portion; and

[0011] an oxygen-impermeable dielectric spacer laterally abutting sidewalls of the high-k material portion and the metal gate portion;

and wherein the semiconductor gate structure includes:

[0012] a semiconductor oxide containing gate dielectric portion having a dielectric constant less than 8.0 and located directly on the semiconductor substrate;

[0013] a doped semiconductor portion comprising a doped semiconductor material and vertically abutting the gate dielectric; and

[0014] a low-k gate spacer comprising a dielectric material having a dielectric constant less than 4.0 and laterally abutting sidewalls of the semiconductor oxide containing gate dielectric portion and the doped semiconductor portion.

[0015] In one embodiment, the high-k material portion further includes a chemical oxide portion vertically abutting the high-k material portion and the semiconductor substrate and comprising an oxide of a semiconductor material of the semiconductor substrate.

[0016] In another embodiment, the oxygen-impermeable dielectric spacer has an L-shaped vertical cross-sectional area and vertically abuts the semiconductor substrate.

[0017] In even another embodiment, the semiconductor structure further comprises another low-k gate spacer abutting the oxygen-impermeable dielectric spacer.

[0018] In yet another embodiment, the oxygen-impermeable dielectric spacer comprises silicon nitride.

[0019] In still another embodiment, the low-k gate spacer comprises silicon oxide.

[0020] In still yet another embodiment, the low-k gate spacer comprises a low-k dielectric material having a dielectric constant less than 2.8.